FIG.1

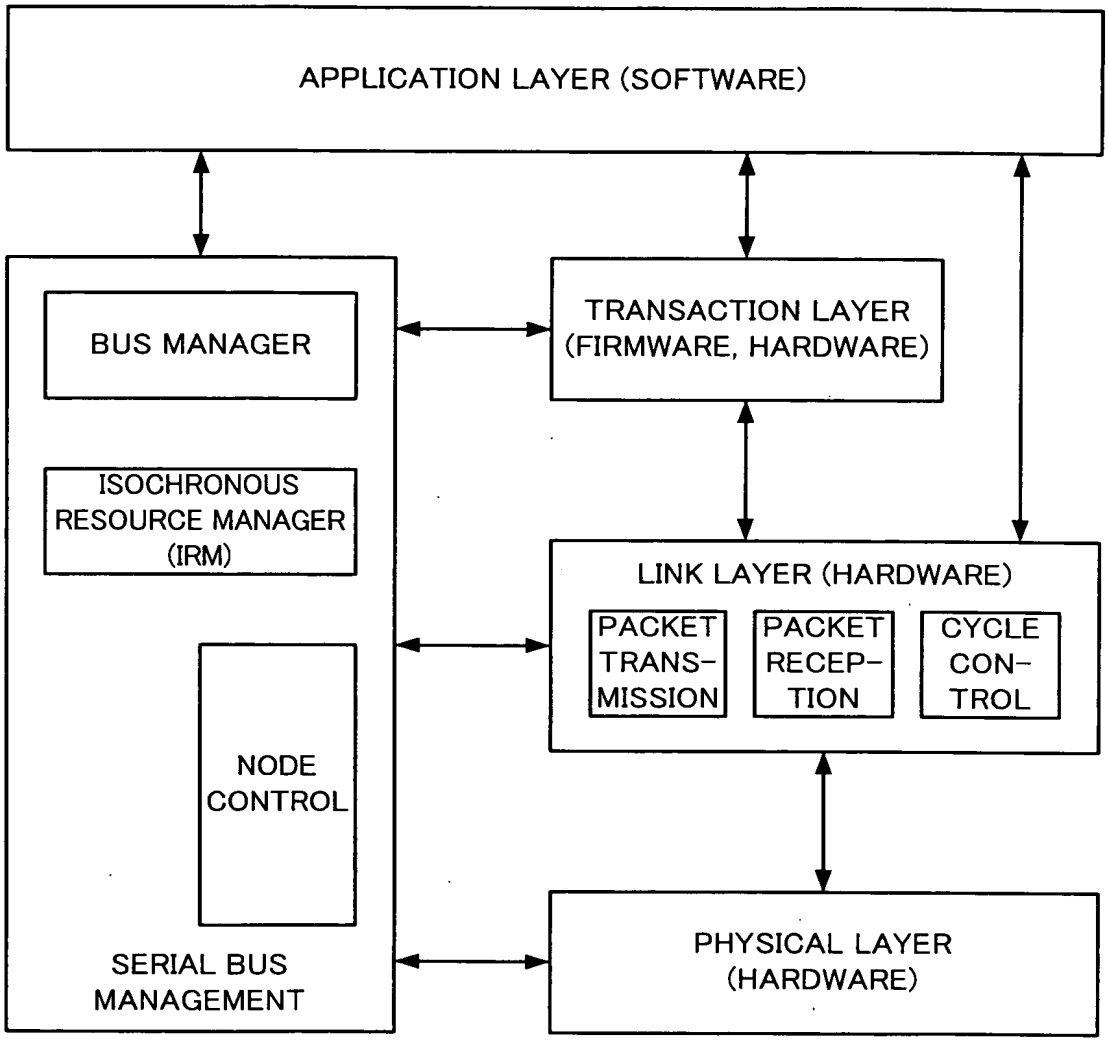

APPLICATION LAYER (SOFTWARE)
BUS MANAGER
ISOCHRONOUS RESOURCE MANAGER (IRM)
NODE CONTROL
SERIAL BUS MANAGEMENT
TRANSACTION LAYER (FIRMWARE, HARDWARE)
LINK LAYER (HARDWARE)
PACKET TRANS-MISSION
PACKET RECEP-TION
CYCLE CON-TROL
PHYSICAL LAYER (HARDWARE)

FIG.2A

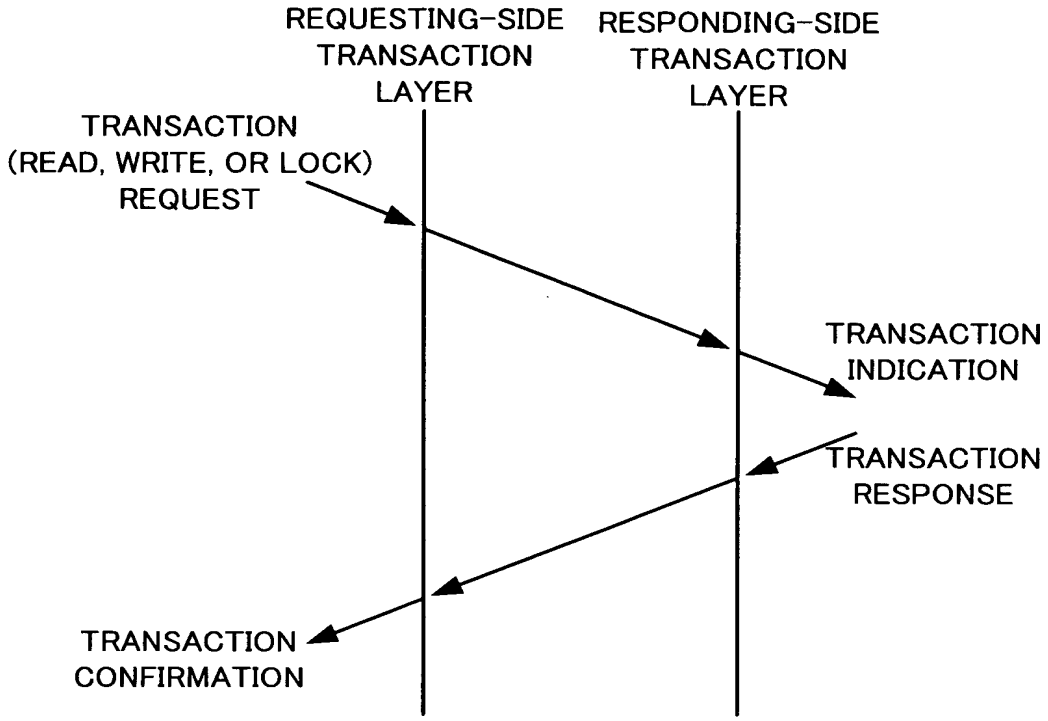

REQUESTING-SIDE TRANSACTION LAYER
RESPONDING-SIDE TRANSACTION LAYER
TRANSACTION (READ, WRITE, OR LOCK) REQUEST
TRANSACTION INDICATION
TRANSACTION RESPONSE
TRANSACTION CONFIRMATION

FIG.2B

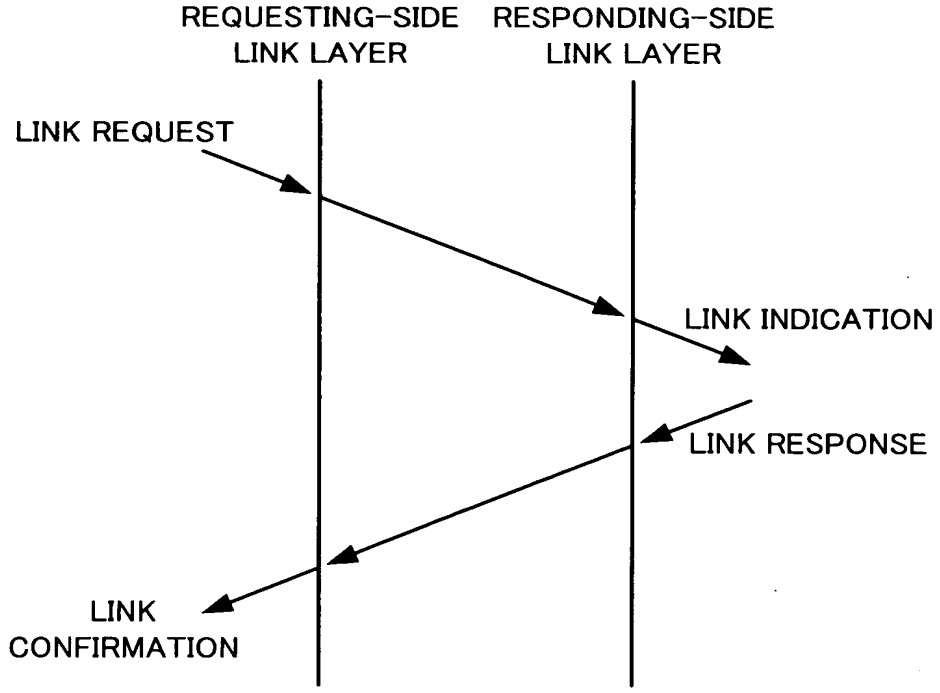
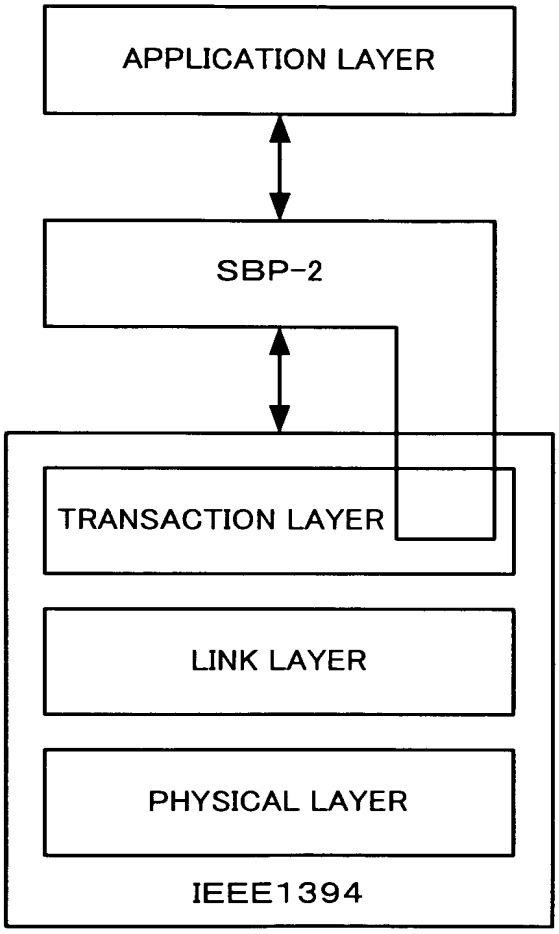

REQUESTING-SIDE LINK LAYER
RESPONDING-SIDE LINK LAYER
LINK REQUEST
LINK INDICATION
LINK RESPONSE
LINK CONFIRMATION

FIG.3


APPLICATION LAYER
SBP-2
TRANSACTION LAYER
LINK LAYER
PHYSICAL LAYER
IEEE1394

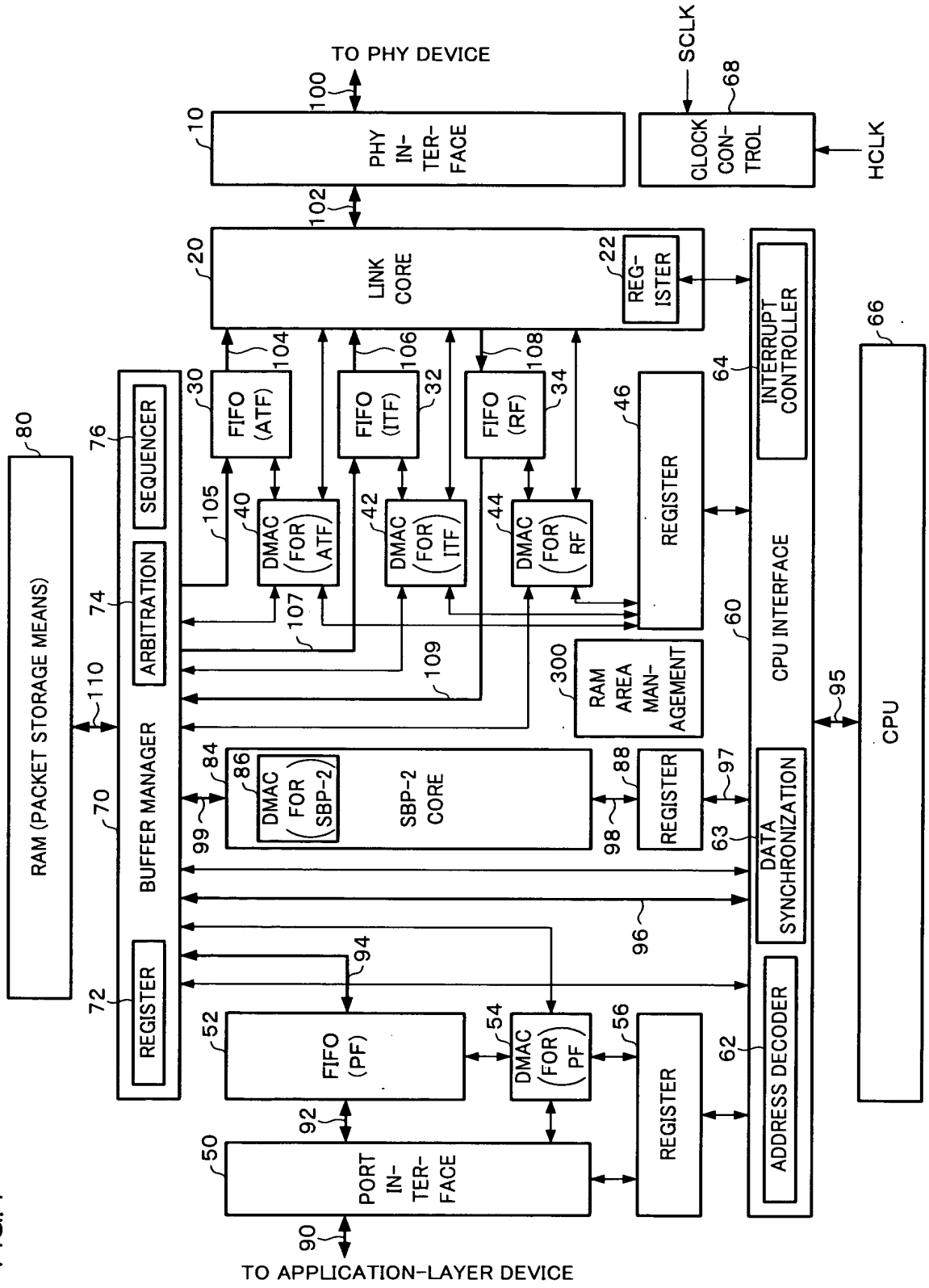
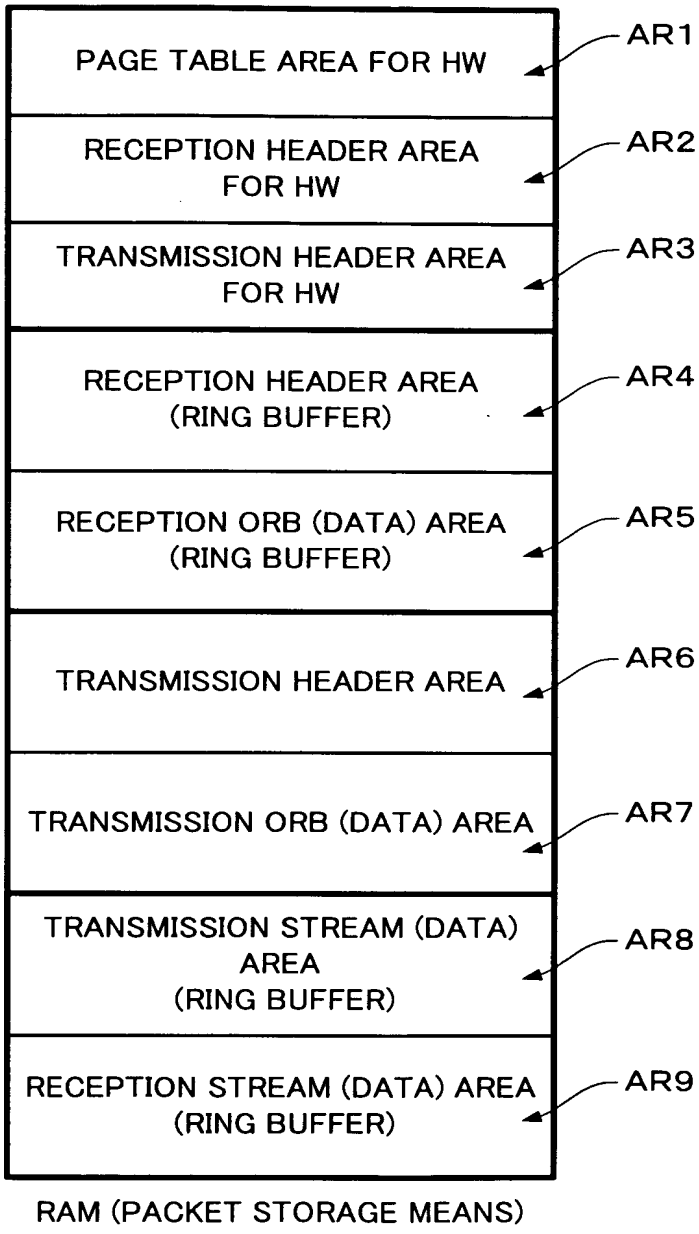

TO PHY DEVICE
SCLK
HCLK
PHY INTERFACE
CLOCK CONTROL
LINK CORE
REGISTER
INTERRUPT CONTROLLER
FIFO (ATF)
FIFO (ITF)
FIFO (RF)
DMAC (FOR ATF)
DMAC (FOR ITF)
DMAC (FOR RF)
REGISTER
RAM (PACKET STORAGE MEANS)
SEQUENCER
ARBITRATION
BUFFER MANAGER
RAM AREA MANAGEMENT
CPU INTERFACE
CPU
DMAC FOR SBP-2
SBP-2 CORE
REGISTER
DATA SYNCHRONIZATION
REGISTER
FIFO (PF)
DMAC (FOR PF)
REGISTER
ADDRESS DECODER
PORT INTERFACE
TO APPLICATION-LAYER DEVICE

FIG.4

FIG.5


PAGE TABLE AREA FOR HW
AR1
RECEPTION HEADER AREA FOR HW
AR2
TRANSMISSION HEADER AREA FOR HW
AR3
RECEPTION HEADER AREA (RING BUFFER)
AR4
RECEPTION ORB (DATA) AREA (RING BUFFER)
AR5
TRANSMISSION HEADER AREA
AR6
TRANSMISSION ORB (DATA) AREA
AR7
TRANSMISSION STREAM (DATA) AREA (RING BUFFER)
AR8
RECEPTION STREAM (DATA) AREA (RING BUFFER)
AR9
RAM (PACKET STORAGE MEANS)

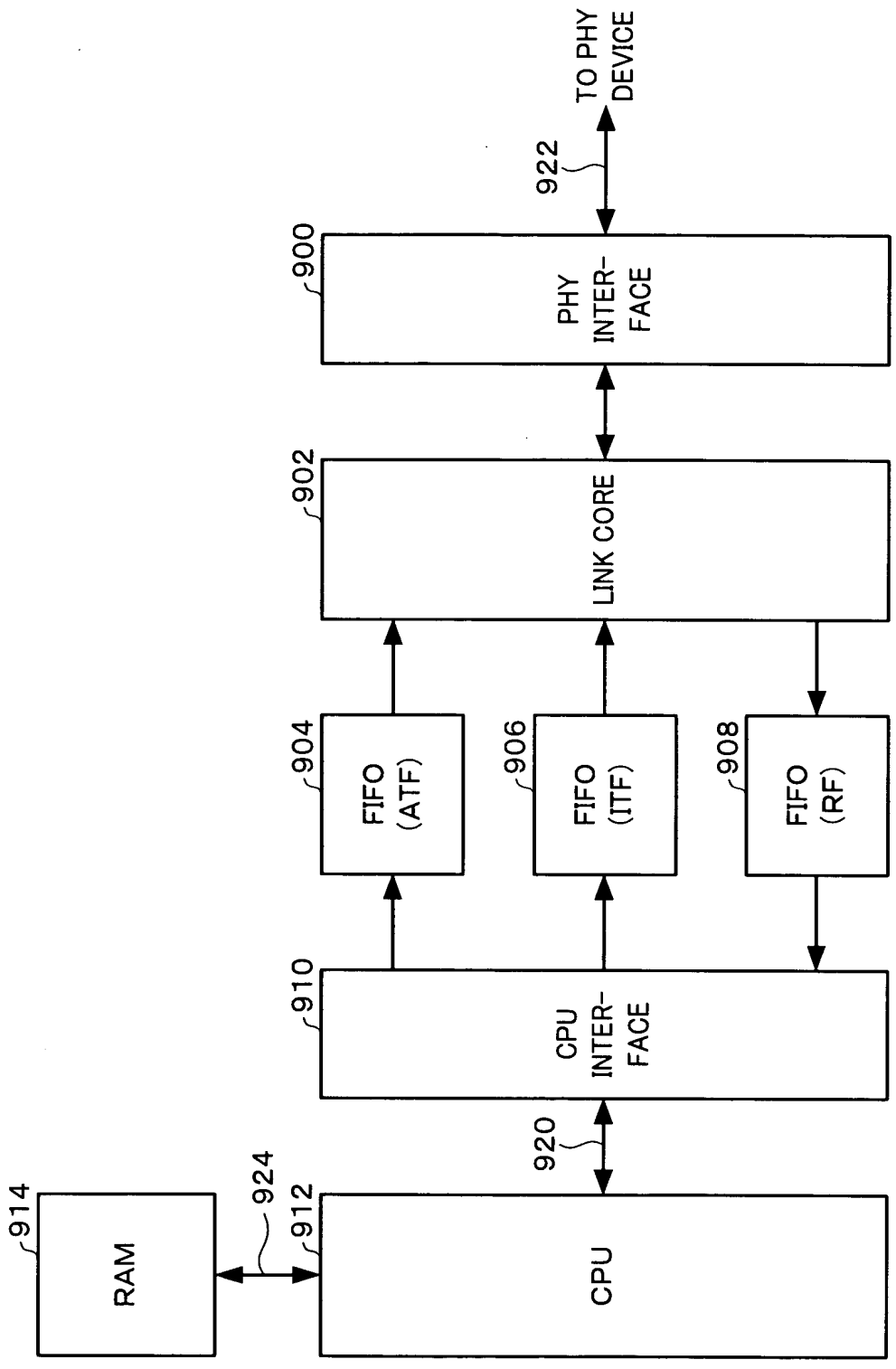

TO PHY DEVICE
922
900
PHY INTER-FACE
902
LINK CORE
904
FIFO (ATF)
906
FIFO (ITF)
908
FIFO (RF)
910
CPU INTER-FACE
920
924
914
RAM
912
CPU

FIG.6

FIG.7

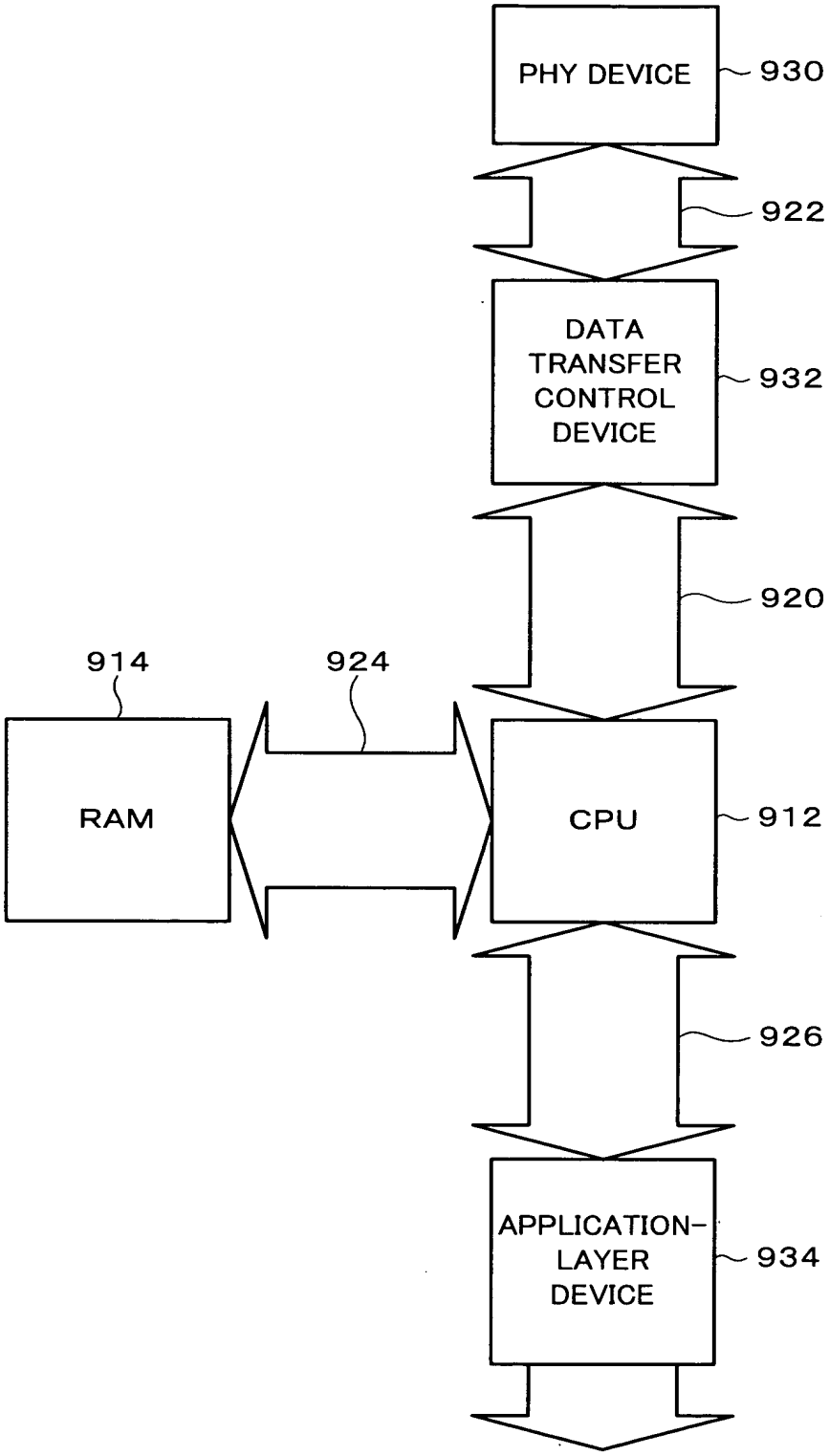

PHY DEVICE
930
922
DATA TRANSFER CONTROL DEVICE
932
920
914
924
RAM
CPU
912
926
APPLICATION-LAYER DEVICE
934

FIG.8

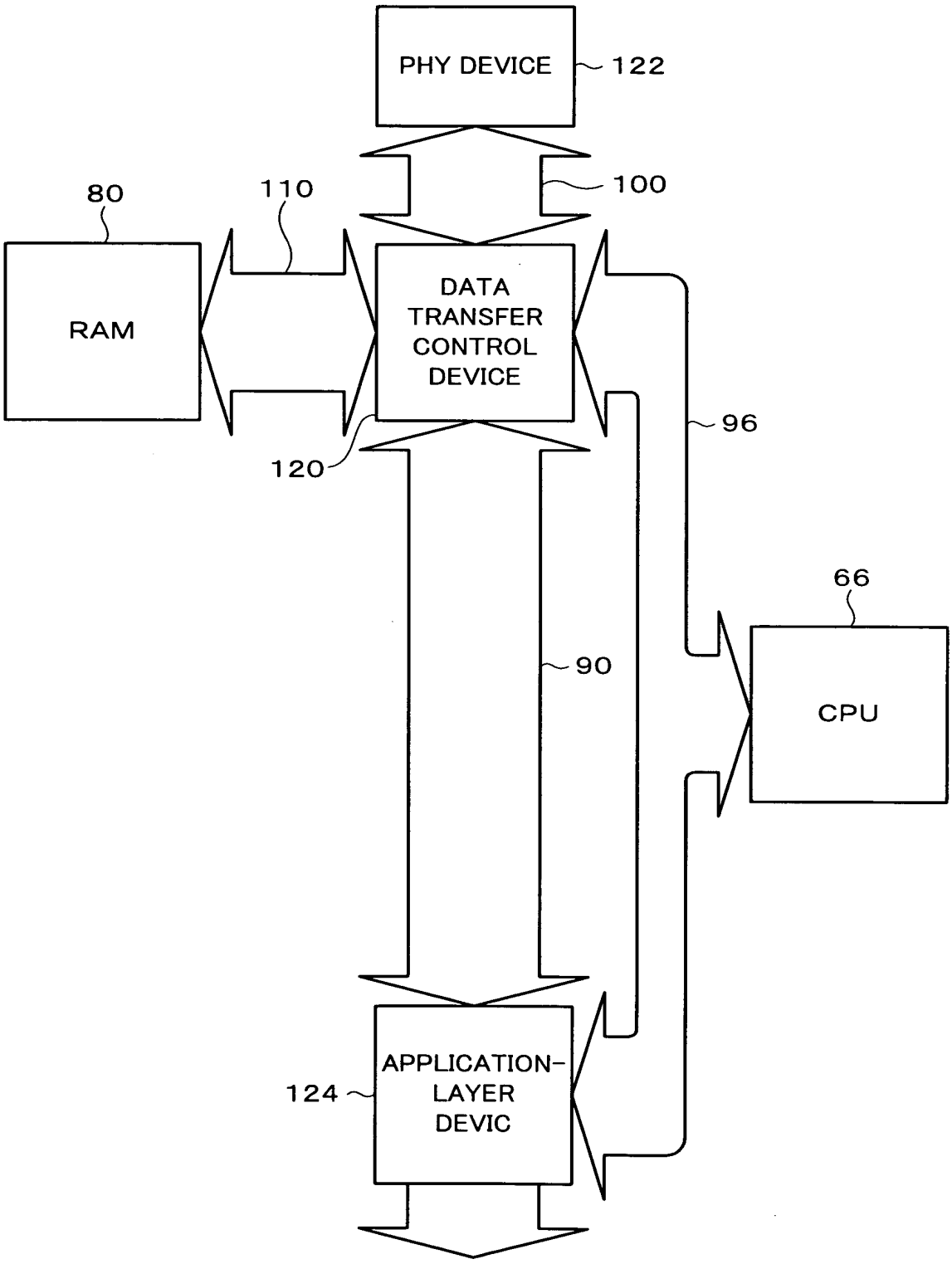

PHY DEVICE
122
80
110
100
RAM
DATA
TRANSFER
CONTROL
DEVICE
96
120
66
90
CPU
APPLICATION-
LAYER
DEVIC
124

FIG.9

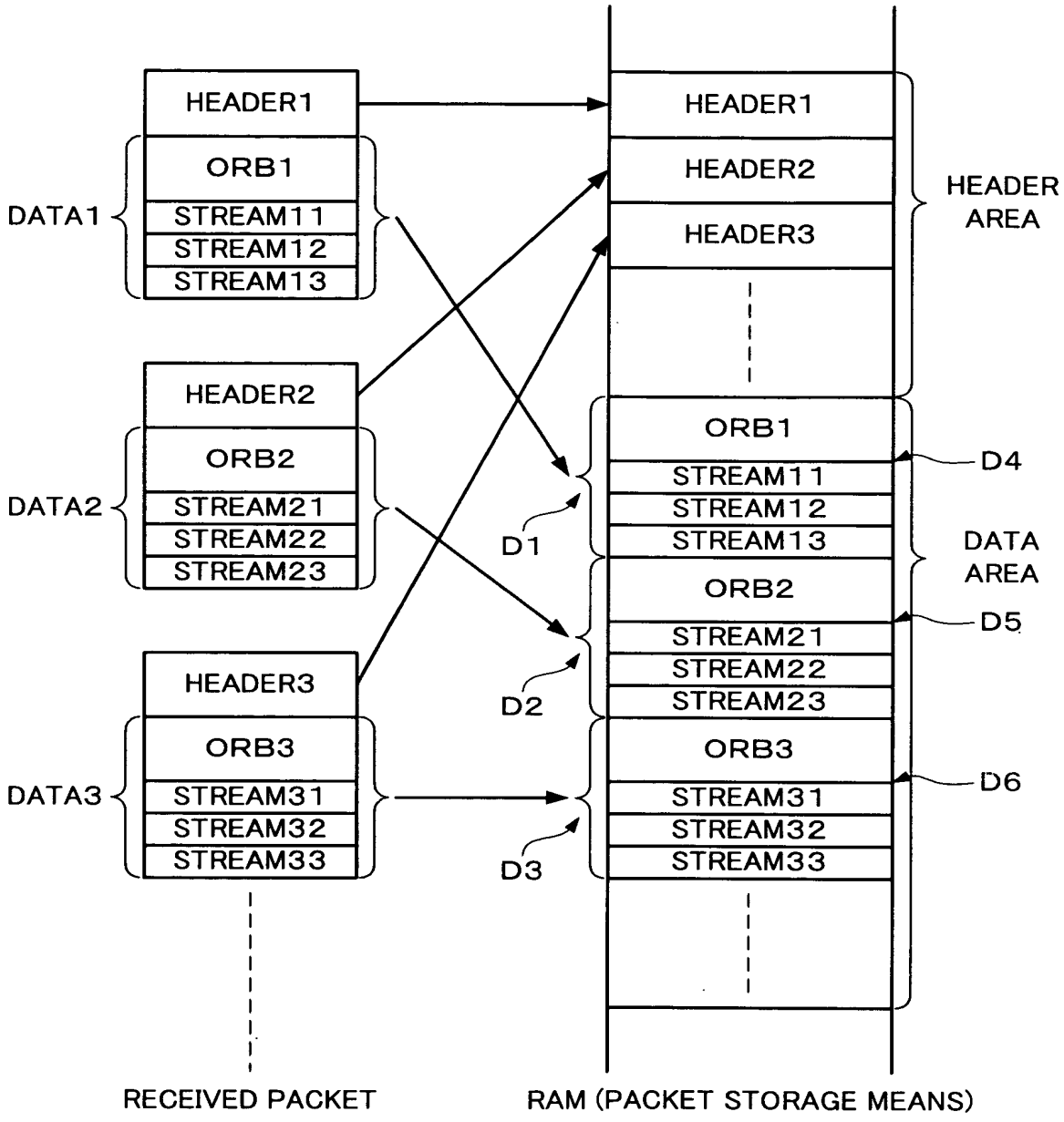
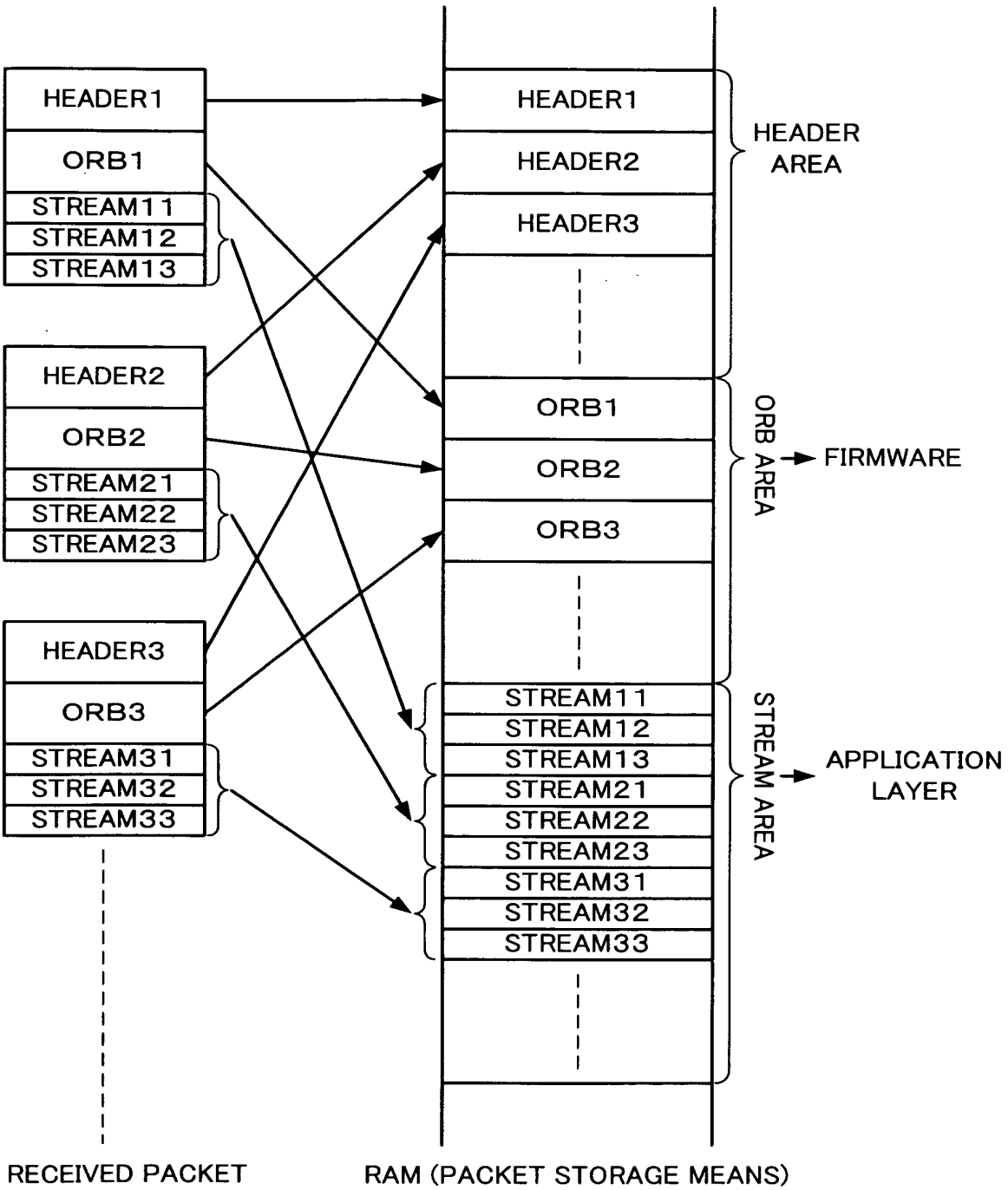

HEADER1
ORB1
DATA1
STREAM11
STREAM12
STREAM13
HEADER2
ORB2
DATA2
STREAM21
STREAM22
STREAM23
HEADER3
ORB3
DATA3
STREAM31
STREAM32
STREAM33
RECEIVED PACKET
HEADER1
HEADER2
HEADER3
HEADER AREA
ORB1
STREAM11
STREAM12
STREAM13
ORB2
STREAM21
STREAM22
STREAM23
ORB3
STREAM31
STREAM32
STREAM33
D1
D2
D3
D4
D5
D6
DATA AREA
RAM (PACKET STORAGE MEANS)

FIG.10


HEADER1
ORB1
STREAM11
STREAM12
STREAM13
HEADER2
ORB2
STREAM21
STREAM22
STREAM23
HEADER3
ORB3
STREAM31
STREAM32
STREAM33
RECEIVED PACKET
HEADER1
HEADER2
HEADER3
ORB1
ORB2
ORB3
STREAM11
STREAM12
STREAM13
STREAM21
STREAM22
STREAM23
STREAM31
STREAM32
STREAM33
RAM (PACKET STORAGE MEANS)
HEADER AREA
ORB AREA
FIRMWARE
STREAM AREA
APPLICATION LAYER

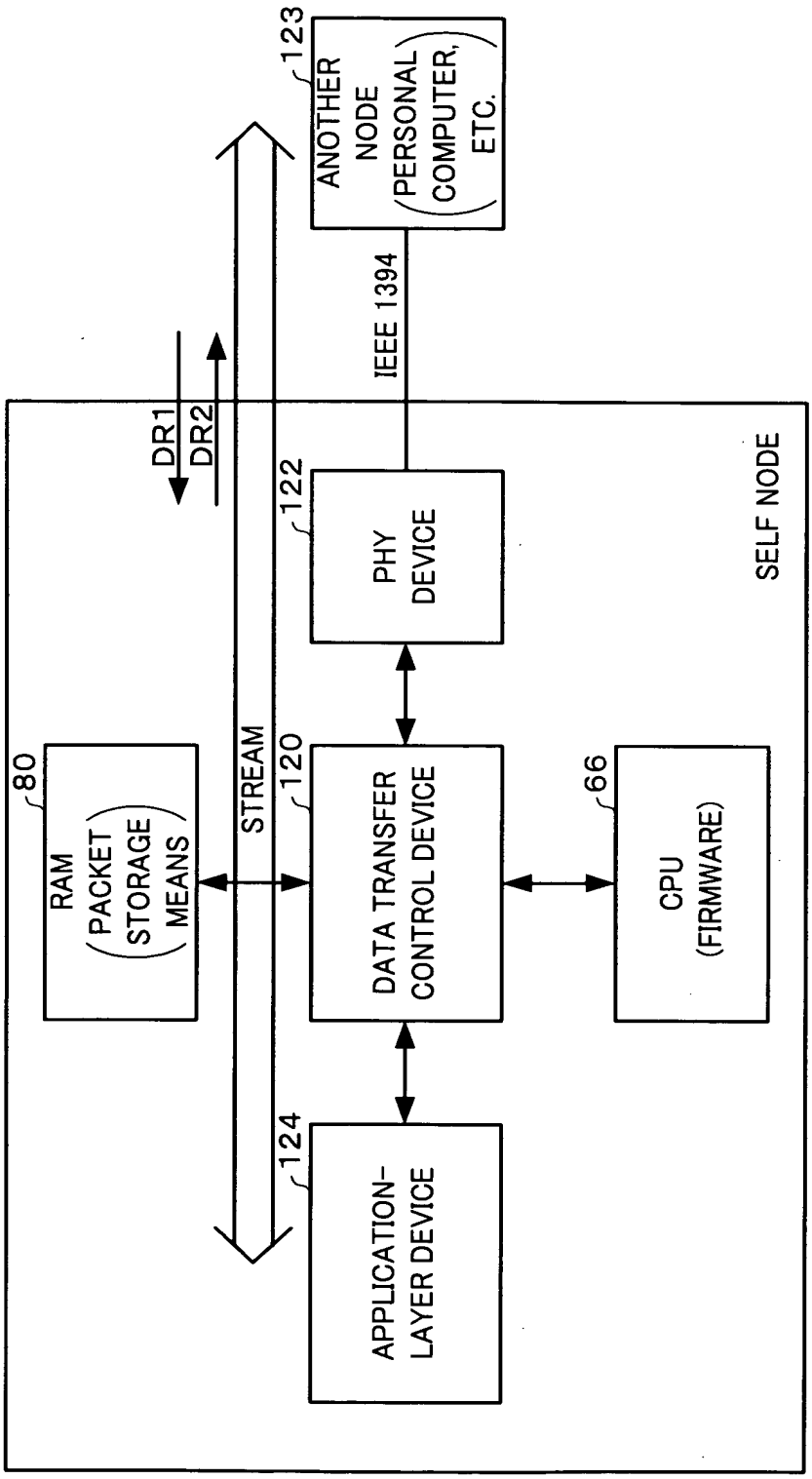

123
ANOTHER NODE (PERSONAL COMPUTER, ETC.)
IEEE 1394
DR1
DR2
122
PHY DEVICE
SELF NODE
80
RAM (PACKET STORAGE MEANS)
STREAM
120
DATA TRANSFER CONTROL DEVICE
66
CPU (FIRMWARE)
124
APPLICATION-LAYER DEVICE

FIG.11

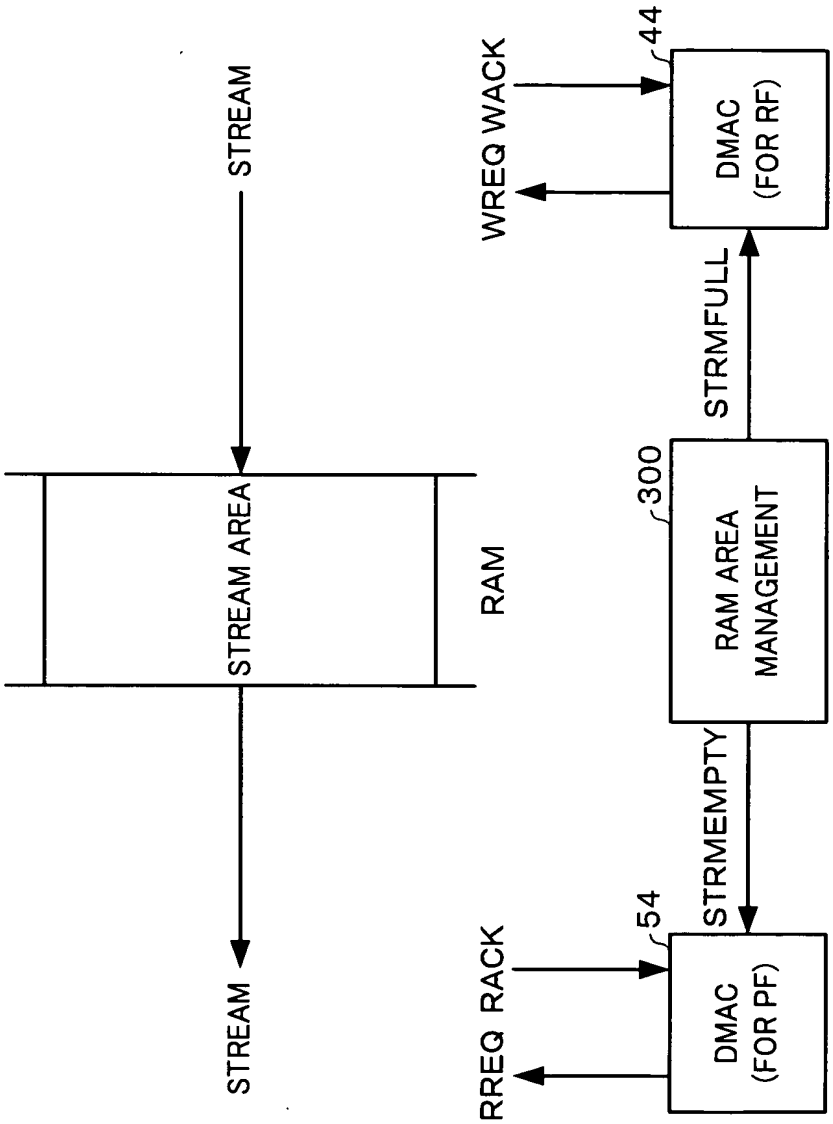

STREAM
STREAM AREA
RAM
STREAM
WREQ WACK
44
DMAC
(FOR RF)
STRMFULL
300
RAM AREA
MANAGEMENT
STRMEMPTY
RREQ RACK
54
DMAC
(FOR PF)

FIG.12

FIG.13A

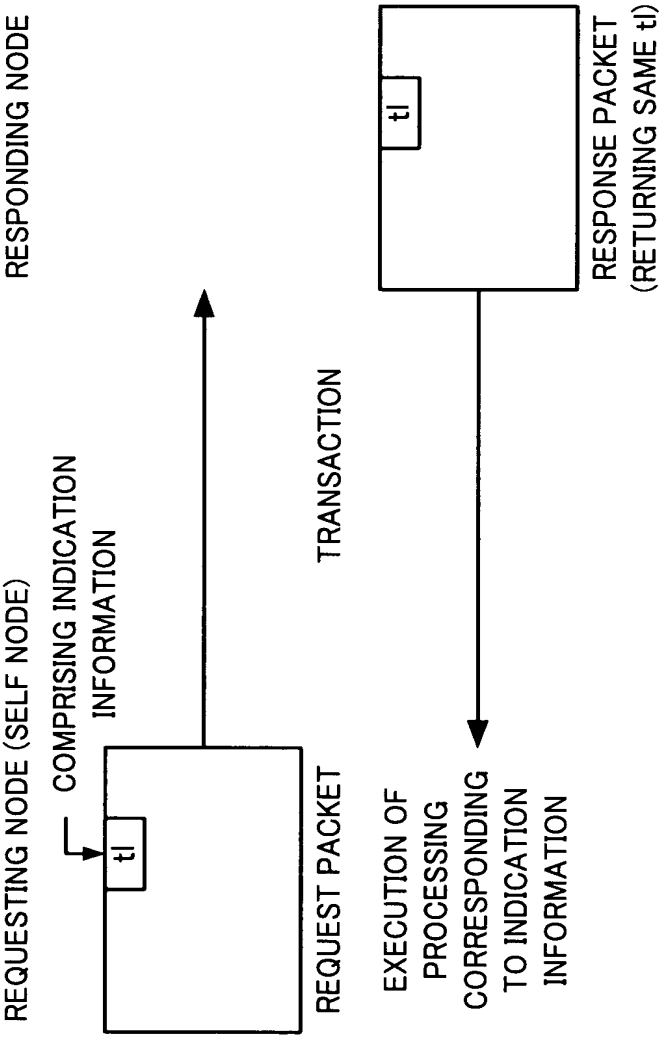


FIG.13B

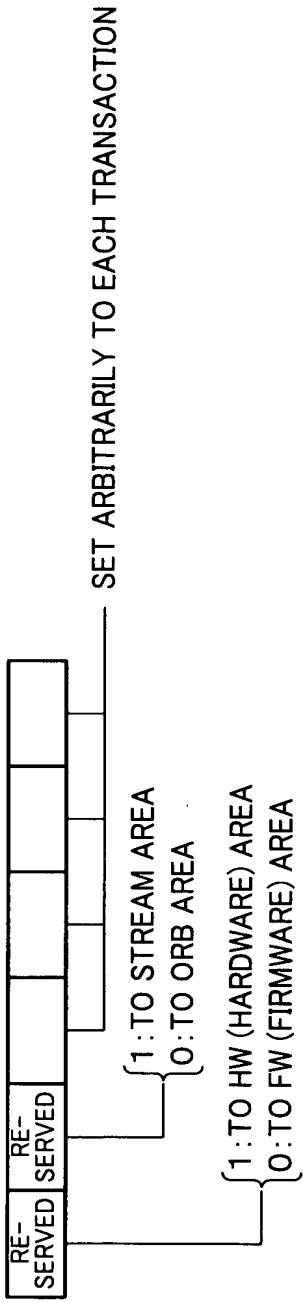


FIG.14

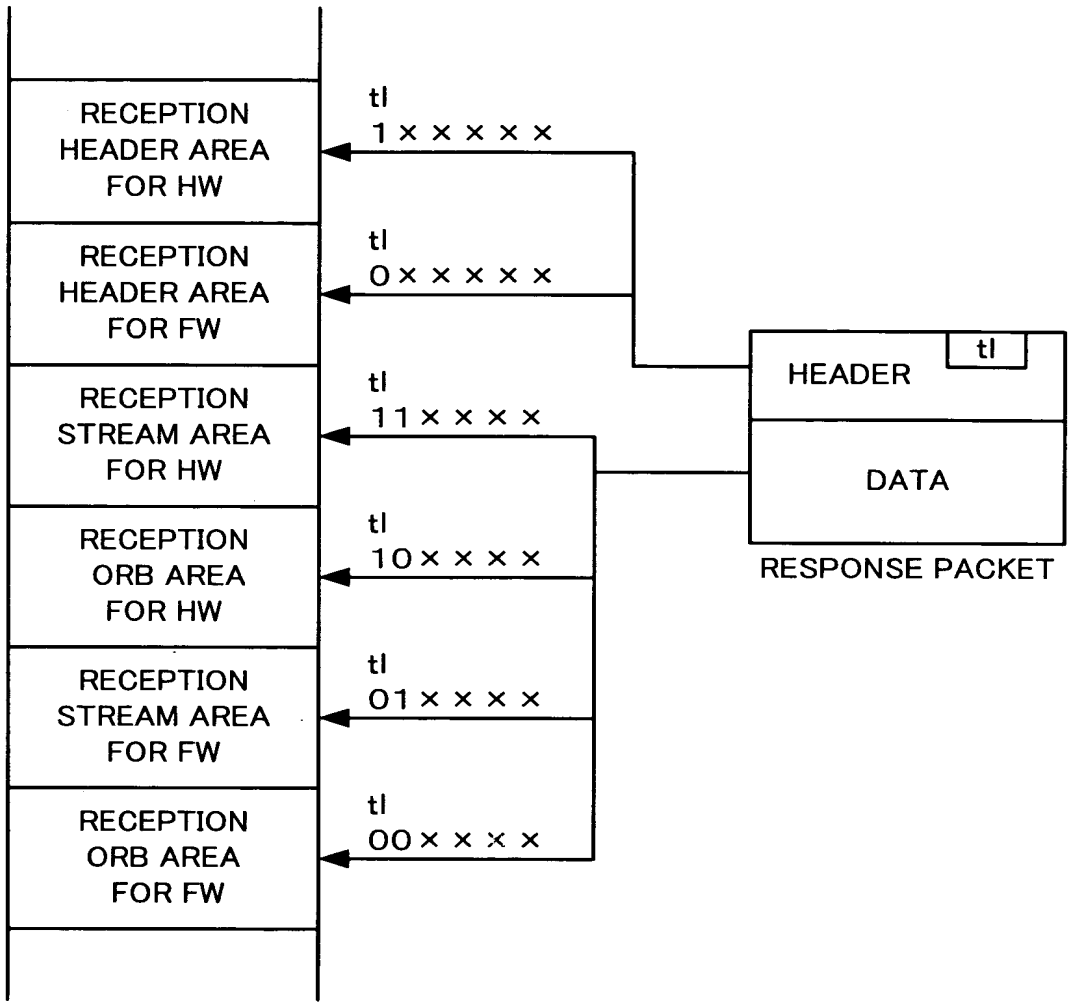

RECEPTION HEADER AREA FOR HW
RECEPTION HEADER AREA FOR FW
RECEPTION STREAM AREA FOR HW
RECEPTION ORB AREA FOR HW
RECEPTION STREAM AREA FOR FW
RECEPTION ORB AREA FOR FW
tl
1×××××
tl
0×××××
tl
11××××
tl
10××××
tl
01××××
tl
00××××
HEADER
tl
DATA
RESPONSE PACKET
RAM (PACKET STORAGE MEANS)

FIG.15

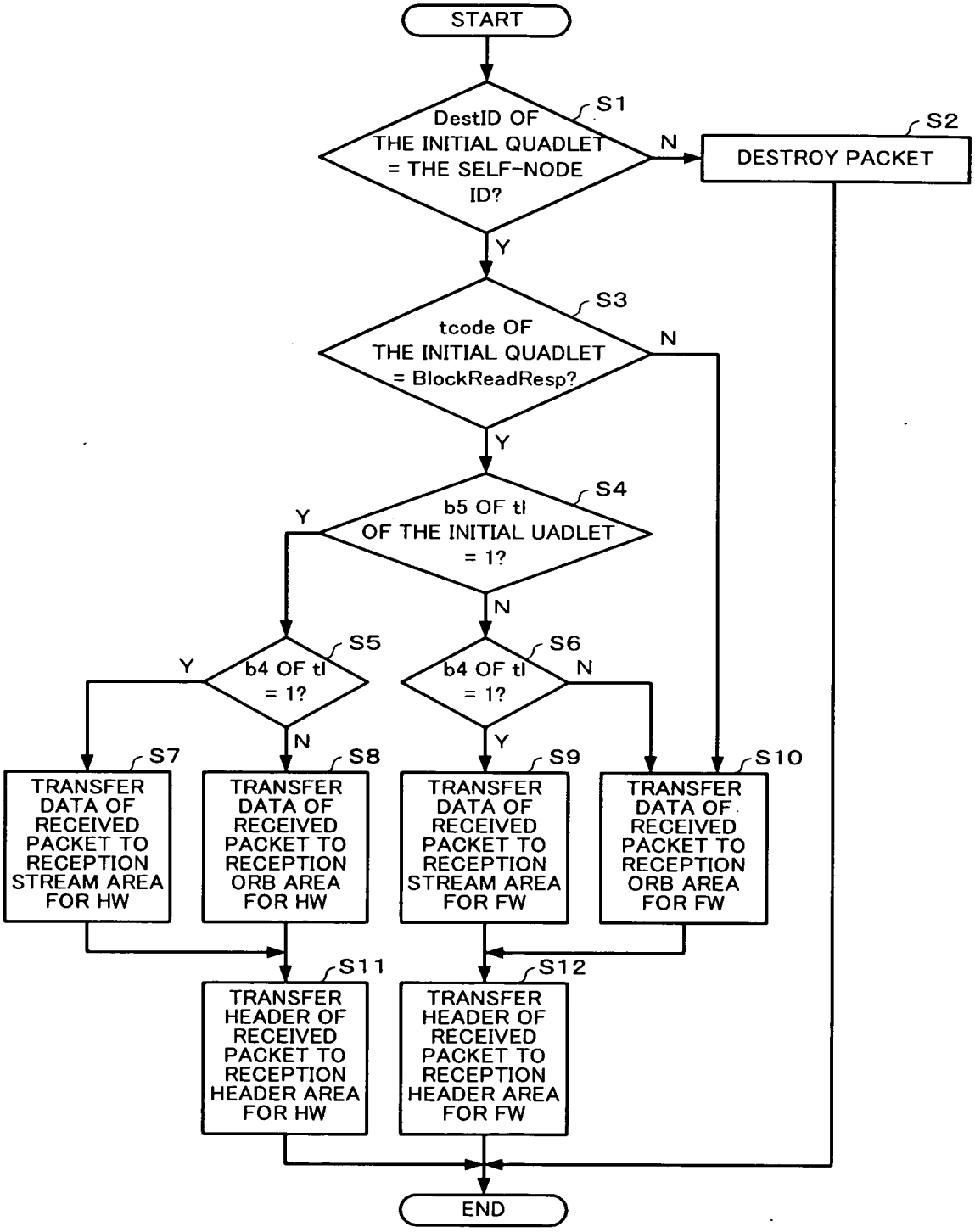

START
DestID OF THE INITIAL QUADLET = THE SELF-NODE ID?
S1
N
S2
DESTROY PACKET
Y
tcode OF THE INITIAL QUADLET = BlockReadResp?
S3
N
Y
b5 OF tl OF THE INITIAL UADLET = 1?
S4
Y
N
b4 OF tl = 1?
S5
Y
N
b4 OF tl = 1?
S6
N
Y
TRANSFER DATA OF RECEIVED PACKET TO RECEPTION STREAM AREA FOR HW
S7
TRANSFER DATA OF RECEIVED PACKET TO RECEPTION ORB AREA FOR HW
S8
TRANSFER DATA OF RECEIVED PACKET TO RECEPTION STREAM AREA FOR FW
S9
TRANSFER DATA OF RECEIVED PACKET TO RECEPTION ORB AREA FOR FW
S10
TRANSFER HEADER OF RECEIVED PACKET TO RECEPTION HEADER AREA FOR HW
S11
TRANSFER HEADER OF RECEIVED PACKET TO RECEPTION HEADER AREA FOR FW
S12
END

FIG.16

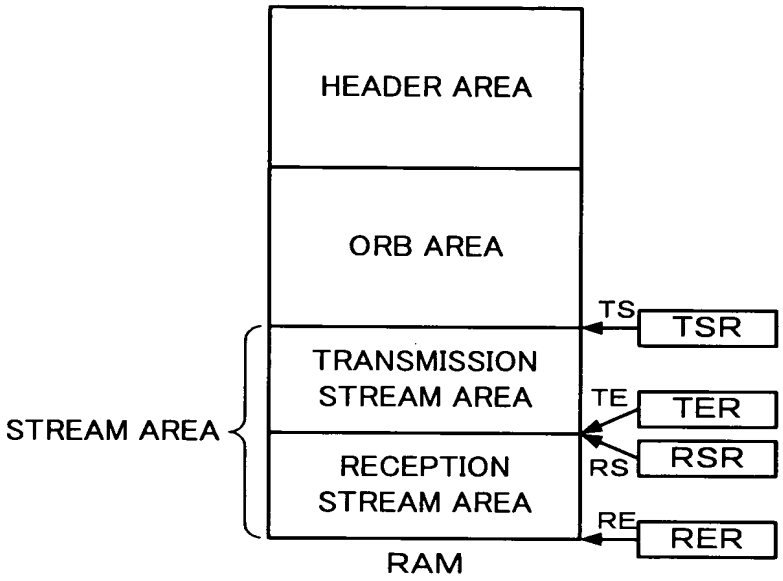

HEADER AREA
ORB AREA
TRANSMISSION STREAM AREA
RECEPTION STREAM AREA
STREAM AREA
RAM
TS
TSR
TE
TER
RS
RSR
RE
RER

FIG.17A

FIRST MODE

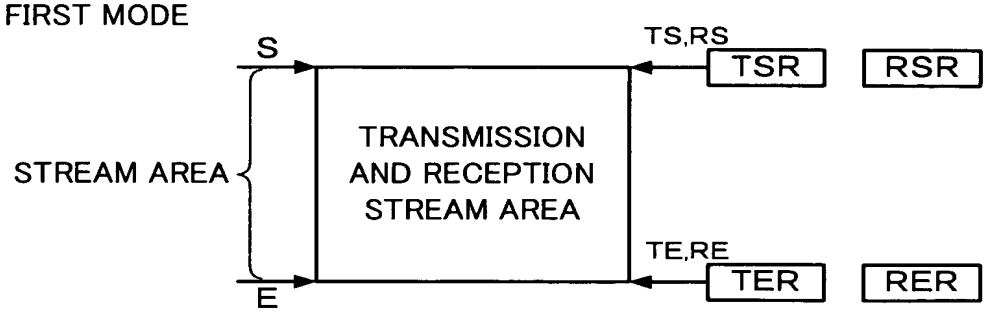


FIG.17B

SECOND MODE

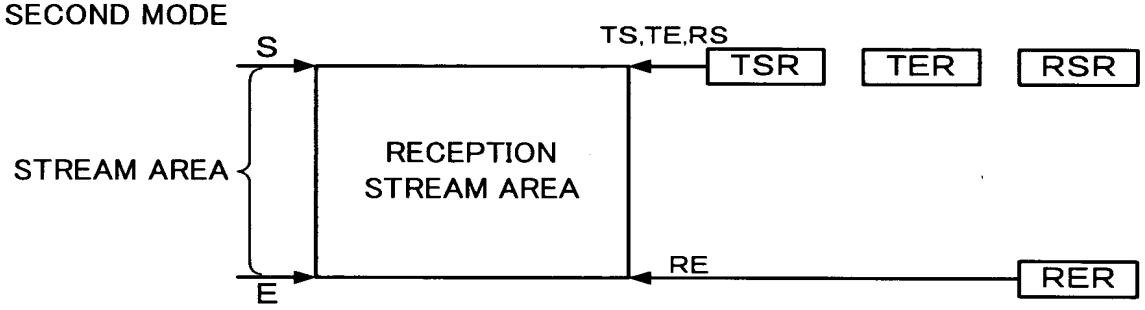


FIG.17C

THIRD MODE

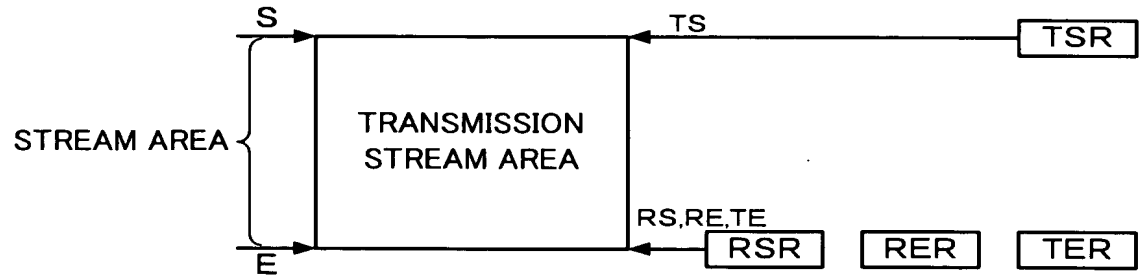


FIG.17D

FOURTH MODE

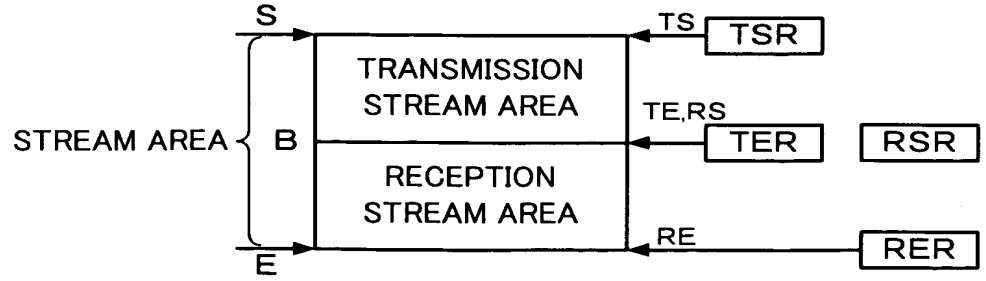
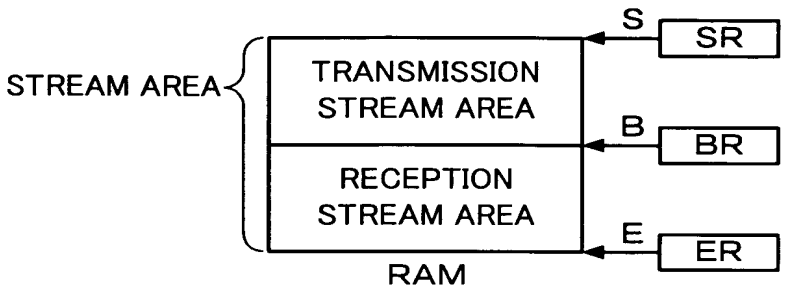


FIG.18


STREAM AREA
TRANSMISSION STREAM AREA
RECEPTION STREAM AREA
RAM
S
SR
B
BR
E
ER

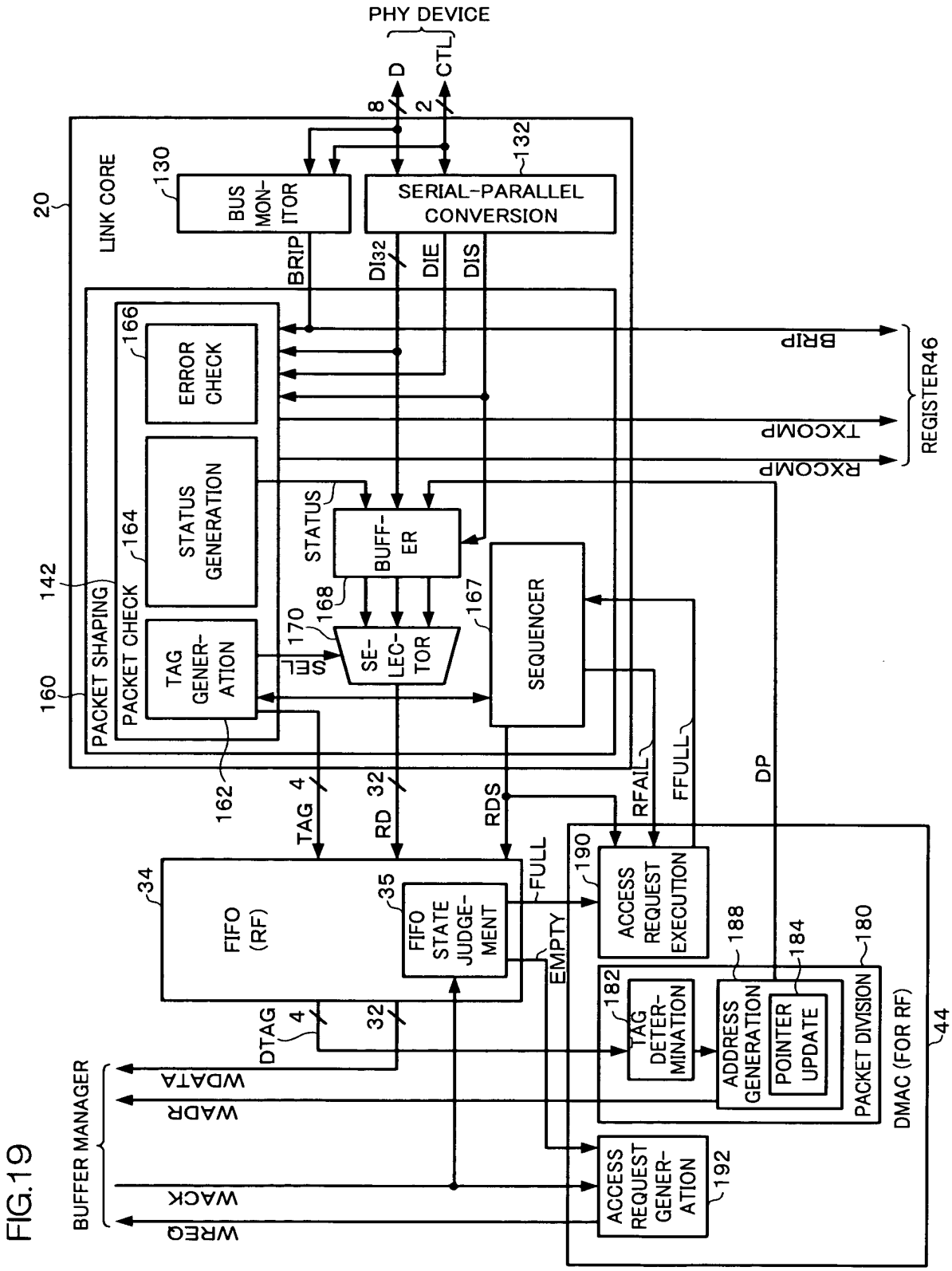

PHY DEVICE
D
CTL
8
2
20
LINK CORE
130
BUS MON-ITOR
132
SERIAL-PARALLEL CONVERSION
BRIP
DI32
DIE
DIS
166
ERROR CHECK
164
STATUS GENERATION
142
PACKET SHAPING
PACKET CHECK
160
TAG GENER-ATION
STATUS
BUFF-ER
168
170
SE-LEC-TOR
167
SEQUENCER
BRIP
TXCOMP
RXCOMP
REGISTER46
162
TAG 4
RD 32
RDS
RFAIL
FFULL
DP
34
FIFO (RF)
35
FIFO STATE JUDGE-MENT
FULL
EMPTY
190
ACCESS REQUEST EXECUTION
188
184
180
182
TAG DETER-MINATION
ADDRESS GENERATION
POINTER UPDATE
PACKET DIVISION
DMAC (FOR RF)
44
DTAG 4
32
BUFFER MANAGER
WDATA
WADR
WACK
WREQ
ACCESS REQUEST GENER-ATION
192

FIG.19

FIG.20A

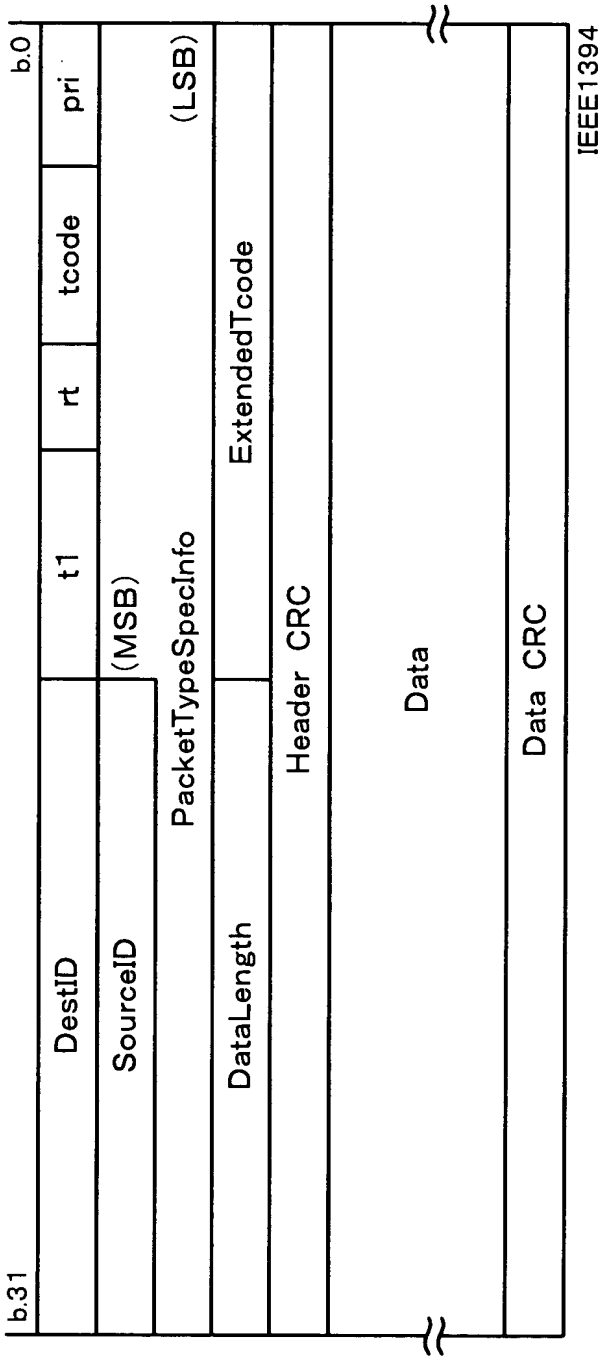


FIG.20B

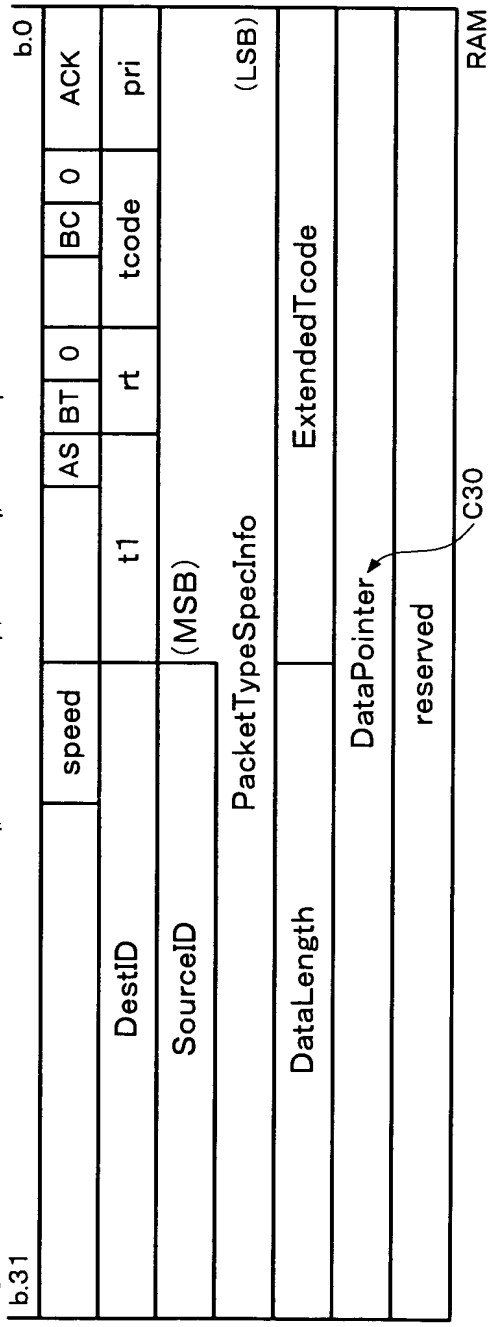


FIG.21

TAG(DTAG)	MEANING
0001	FW−SOP
0010	FW−HDR
0011	FW−FTR
0100	FW−ORB
0101	FW−STRM
1001	HW−SOP
1010	HW−HDR
1011	HW−FTR
1100	HW−ORB
1101	HW−STRM

FW ····· FIRMWARE
HW ····· HARDWARE
SOP ····· START OF PACKET
(INITIAL QUADLET OF RECEIVED PACKET)
HDR ····· HEADER OTHER THAN SOP
FTR ····· ACK TRANSMISSION
ORB ····· ORB (DATA)
STRM ····· STREAM (DATA)

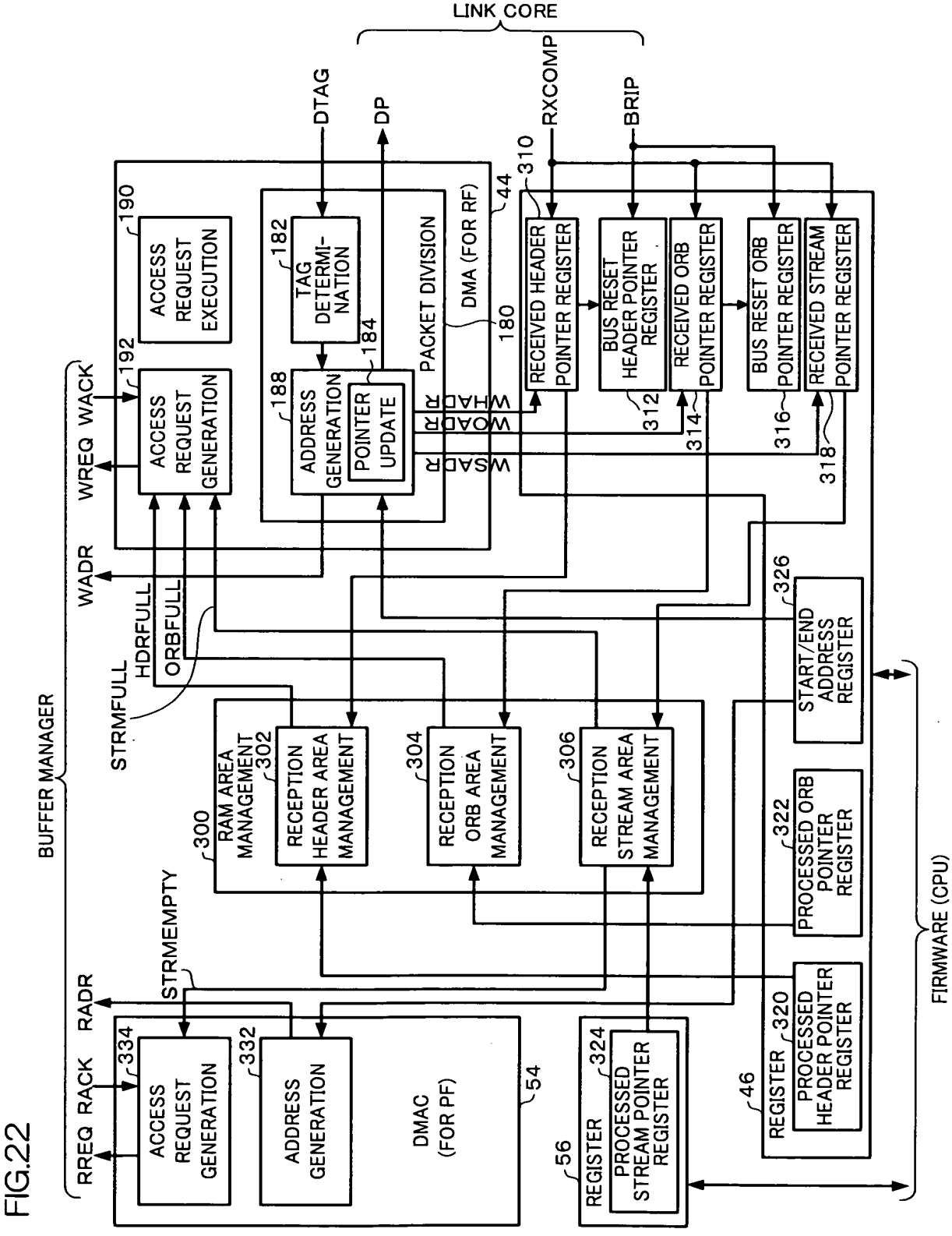

LINK CORE
DTAG
DP
RXCOMP
BRIP
310
44
190
ACCESS REQUEST EXECUTION
182
TAG DETERMI-NATION
184
PACKET DIVISION
DMA (FOR RF)
180
RECEIVED HEADER POINTER REGISTER
BUS RESET HEADER POINTER REGISTER
RECEIVED ORB POINTER REGISTER
BUS RESET ORB POINTER REGISTER
RECEIVED STREAM POINTER REGISTER
192
ACCESS REQUEST GENERATION
188
ADDRESS GENERATION
POINTER UPDATE
HAD
OAD
SAD
312
314
316
318
WREQ
WACK
WADR
HDRFULL
ORBFULL
STRMFULL
326
START/END ADDRESS REGISTER
BUFFER MANAGER
300
RAM AREA MANAGEMENT
302
RECEPTION HEADER AREA MANAGEMENT
304
RECEPTION ORB AREA MANAGEMENT
306
RECEPTION STREAM AREA MANAGEMENT
322
PROCESSED ORB POINTER REGISTER
STRMEMPTY
RADR
RREQ
RACK
334
ACCESS REQUEST GENERATION
332
ADDRESS GENERATION
DMAC (FOR PF)
54
56
REGISTER
324
PROCESSED STREAM POINTER REGISTER
46
REGISTER
320
PROCESSED HEADER POINTER REGISTER
FIRMWARE (CPU)

FIG.22

FIG.23

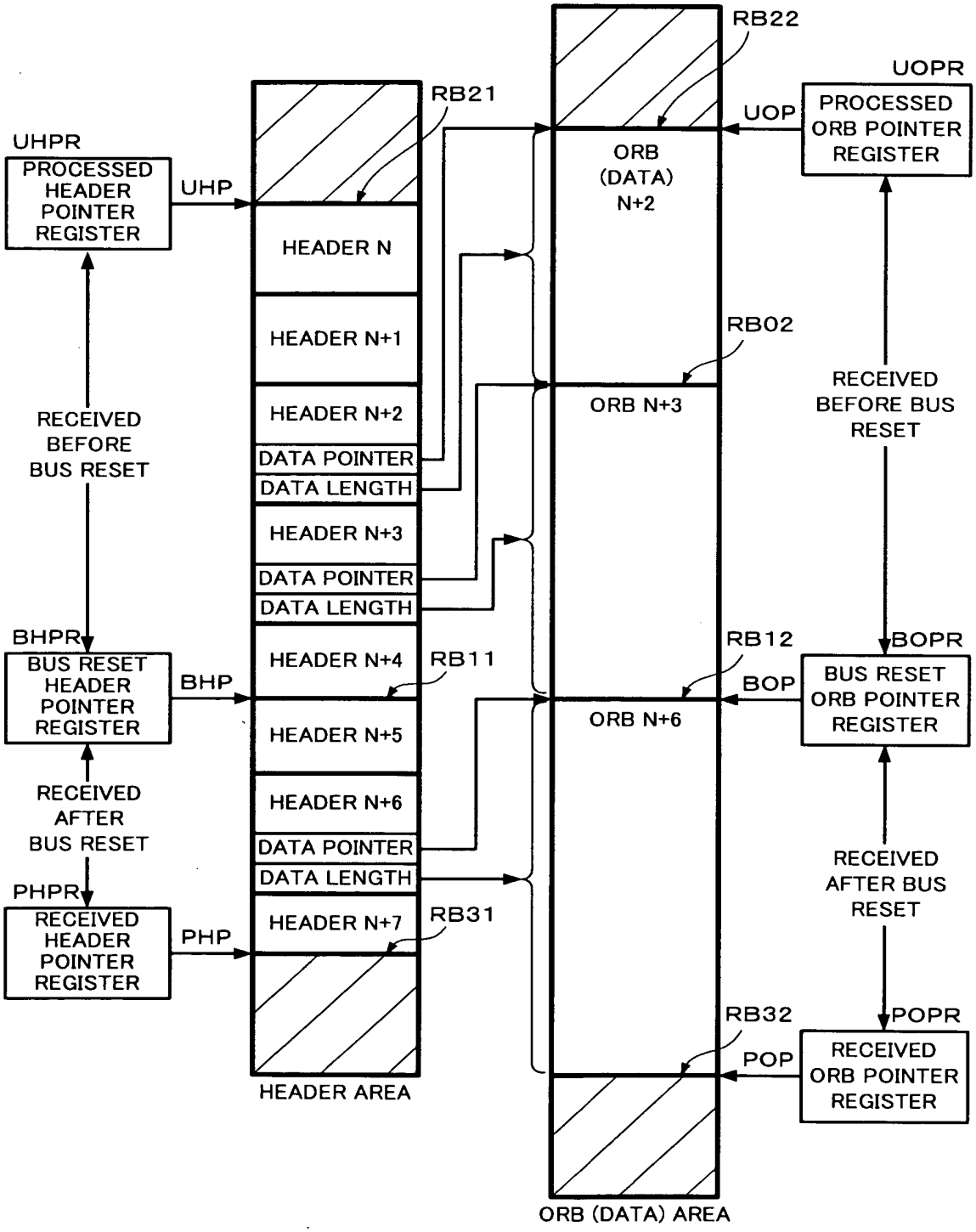

RB22
UOPR
RB21
UOP
PROCESSED ORB POINTER REGISTER
UHPR
PROCESSED HEADER POINTER REGISTER
UHP
ORB (DATA) N+2
HEADER N
HEADER N+1
RB02
HEADER N+2
ORB N+3
RECEIVED BEFORE BUS RESET
RECEIVED BEFORE BUS RESET
DATA POINTER
DATA LENGTH
HEADER N+3
DATA POINTER
DATA LENGTH
BHPR
RB12
BOPR
BUS RESET HEADER POINTER REGISTER
BHP
HEADER N+4
RB11
BOP
BUS RESET ORB POINTER REGISTER
HEADER N+5
ORB N+6
HEADER N+6
RECEIVED AFTER BUS RESET
RECEIVED AFTER BUS RESET
DATA POINTER
DATA LENGTH
PHPR
RECEIVED HEADER POINTER REGISTER
PHP
HEADER N+7
RB31
RB32
POPR
POP
RECEIVED ORB POINTER REGISTER
HEADER AREA
ORB (DATA) AREA

FIG.24A

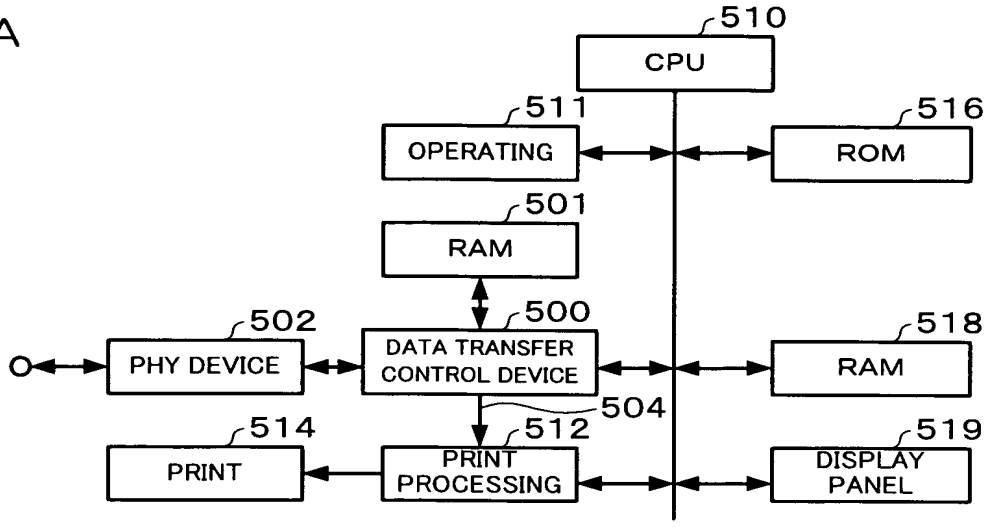


FIG.24B

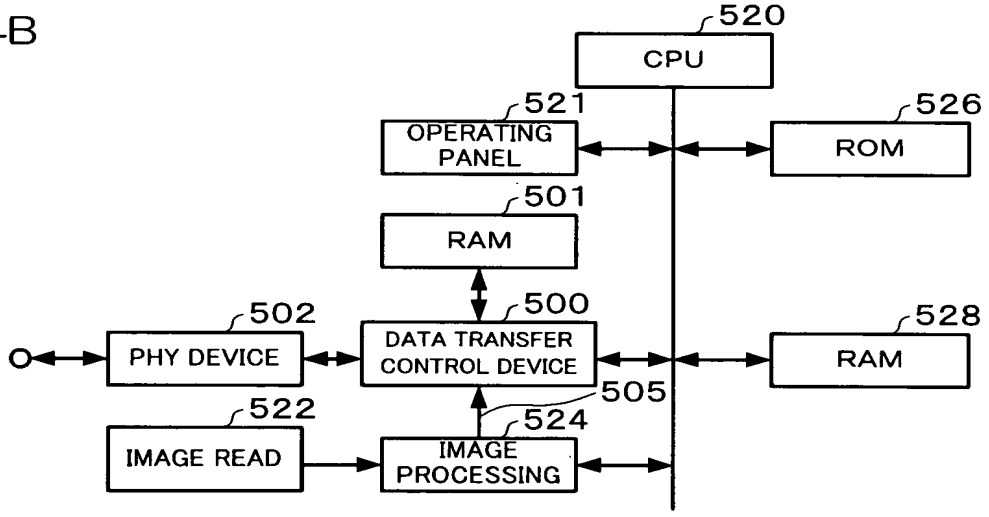


FIG.24C

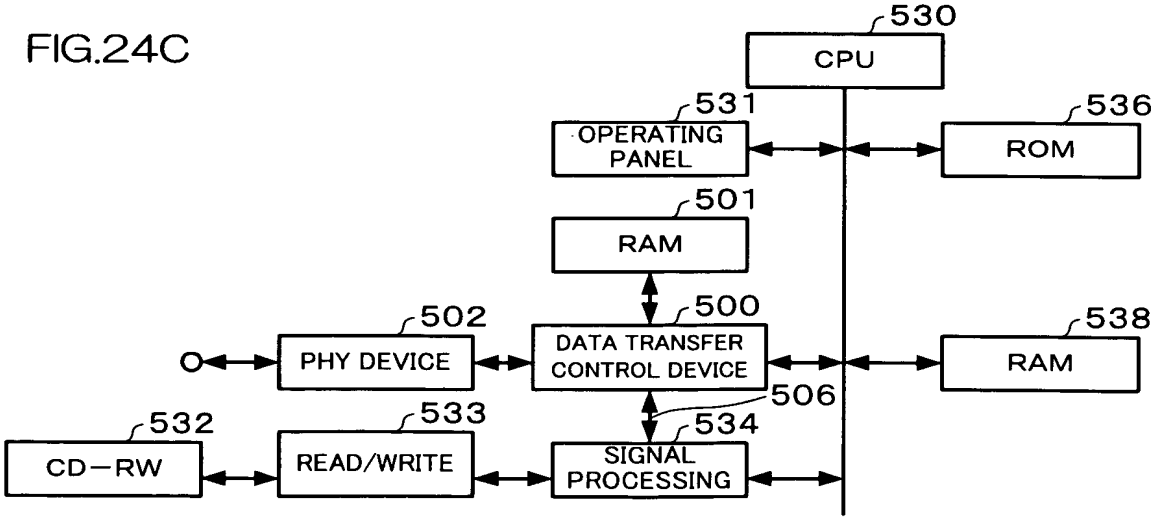


FIG.25A

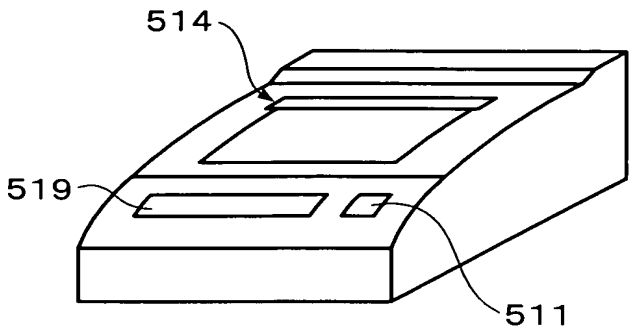


FIG.25B

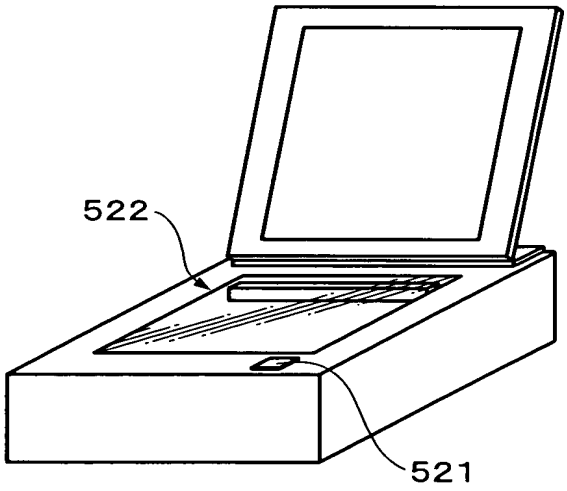


FIG.25C